TRANSMITTAL OF APPEAL BRIEF (Large Entity) POU920000092US1 Management and Man et al. **Group Art Unit** Examiner Filing Date Serial No. 2127 07/18/2000 M. Banankhah 09/618,920 Invention: JOB SCHEDULING BASED UPON AVAILABILITY OF REAL AND/OR VIRTUAL RESOURCES TO THE COMMISSIONER FOR PATENTS: Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on March 15, 2004 RECEIVED The fee for filing this Appeal Brief is: \$330.00 MAY 2 1 2004 Technology Center 2100 A check in the amount of the fee is enclosed. The Director has already been authorized to charge fees in this application to a Deposit Account. X The Director is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. 09-0463

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Dated: MAY 17, 2004

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Mail Stop Appeal Brief - Patents

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Susan L. Phelps

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicant: Chan et al. :
Serial No.: 09/618,920 :

Group Art Unit: 212' Examiner: M. Banankhah

<u>Serial No.: 09/618,920</u> <u>Filed: July 18, 2000</u>

May 17, 2004

Title: JOB SCHEDULING BASED UPON

Lawrence D. Cutter IBM Corporation

AVAILABILITY OF REAL AND/OR VIRTUAL RESOURCES

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APPEAL BRIEF UNDER 37 C. F. R. § 1.192

Hon. Commissioner for Patents Mail Stop Appeal Brief-Patents P.O. Box 1450 Alexandria, VA 22313-1450

Dear Sir:

This is an appeal from a final rejection dated January 23, 2004, rejecting Claims 1-4 of the above-identified patent application. This brief is accompanied by a transmittal letter authorizing the charging of appellants' deposit account for payment of the requisite fees set forth in 37 C.F.R. § 1.17(c).

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I. REAL PARTY IN INTEREST

This application is assigned to International Business Machines Corporation by virtue of an assignment executed on July 18, 2000, by the co-inventors herein and recorded with the United States Patent and Trademark Office at reel 010998, frame 0919 on July 18, 2000. Therefore, the real party in interest herein is International Business Machines Corporation.

II. RELATED APPEALS AND INTERFERENCES

To the knowledge of the appellants, appellants' undersigned legal representative, and the assignee, there are no other appeals or interferences which will directly affect or be directly affected by or have any bearing on the board's decision in the present appeal.

III. STATUS OF CLAIMS

This patent application was filed on July 18, 2000, with the United States Patent and Trademark Office via Express Mail. Following a final rejection dated December 15, 2003, the present applicants submitted a response under 37 C.F.R. § 1.116 on January 23, 2004. Accordingly, applicants' response under 37 C.F.R. § 1.116 was timely submitted and within the two-month requirements set forth in the regulations.

Applicants' attorney called the Examiner on March 11, 2004, inquiring as to the status of the advisory action, and he was told that an advisory action was issued on March 8, 2004, but not necessarily that it had been sent. Nonetheless, an advisory action was finally received on March 15, 2004, having been mailed from the Patent and Trademark Office on March 10, 2004. Applicants accordingly submitted a notice of appeal on March 15, 2004, with an indication of certified deposit with the U.S. Postal Service on that date. In the advisory action, the Examiner indicated that the amendments proposed in applicants' submittal under 37 C.F.R. § 1.116 would be entered for the

<u>purposes of appeal</u>. Accordingly, the claims as listed at the end of the present brief reflect the claims as amended in the Rule 1.116 response.

Briefly then, it is noted that all of applicants' Claims 1-4 are currently rejected and that, for purposes of appeal, the modifications made to applicants' claims in the aforementioned Rule 1.116 response are included in the claims at the end of the present brief. Furthermore, no claims have been indicated as being allowed, no claims have been canceled, and no claims have been objected to.

IV. STATUS OF AMENDMENTS

As indicated above, for purposes of appeal, applicants' amendments made in the Rule 1.116 response submitted on January 23, 2004, will be entered in accordance with the Examiner's indication in the advisory action dated March 10, 2004.

V. SUMMARY OF THE INVENTION

The present invention is generally directed to systems and methods for scheduling jobs running on data processing systems with multiple processors. Conventionally, operating systems running on these processors scheduled jobs to run based upon job descriptions that are provided by system users. The present invention departs from this mode of operation by providing mechanisms which permit much greater user involvement in the selection and control of data processing system resources. The present invention functions by providing a consistent resource model which extends across multiple data processing systems levels. In particular, in applicants' claimed invention, these levels include a hardware level, an operating system level, an administrative system level, and finally a user level. The resource model employed in applicants' invention includes the designation of resources at these various levels both in terms of type and quantity. The model is invoked through the utilization of application program interface-like statements which are analyzed to

determine the requested resource usage. The analyzed statements are then used to schedule and run jobs which use the specified resources.

In applicants' claimed method, resources are defined to multiprocessors in a data processing system. This definition includes a quantity and type associated with that resource. The quantity is typically indicative of resource capacity. The resource also possesses a level designation ranging all the way from the aforementioned hardware level all the way up to the application or user level. Accordingly, in the present invention, resources are characterized by type and resource capacity and additionally also by the level within the data processing system at which the particular resource is present. In applicants' claimed process, it is determined whether an application level user has requested the use of one of these defined resources. The system then determines the availability among the multiple processors as to level, type, and quantity. Lastly, the user job is dispatched along with the requested resources which are indicated as being available at the level and in the type and quantity requested.

Accordingly, the present applicants' have provided a system which permits application level users much greater control over the selection of data processing systems' resources which are to be used in conjunction with the submitted job to be scheduled. The power and flexibility of the present invention derives from the fact that a range of resource types is modeled in a consistent fashion across a number of data processing system levels particularly with respect to the incorporation of type, quantity specifications, and in the modeling of a large variety of resources which are now accessible to application level users. Accordingly, in the method of the present invention, these application level users are afforded much greater flexibility in terms of selection of data processing system resources at a plurality of levels. In particular, it is the incorporation of the ability to select from resources at different levels that sets the applicants' claimed invention apart from the cited art.

VI. ISSUES

- (1) Whether or not applicants' Claims 1-4 are patentable under 35 U.S.C. § 102 when considered in light of the patent to Jones et al. (U.S. Patent No. 6,282,561 issued August 28, 2001, and having an application filing date of December 7, 1995).
 - (2) Whether applicants' Claims 1-4 may be rejected under 35 U.S.C. § 112.

VII. GROUPING OF CLAIMS

No claim grouping is asserted.

VIII. ARGUMENT

A. Rejection Under 35 U.S.C. § 102

With respect to applicants' Claim 1, for example, it is noted that there is contained therein recitations indicating that the resource also has "a level selected from the group consisting of hardware level, operating system level, administrative system level and application level." The notion of resource levels is a concept which is completely missing from the patent to Jones et al. While Jones et al. appear to describe a resource management mechanism for real-time application programs, there is no teaching, disclosure, or suggestion therein that different options may be presented to a user based upon the level at which a resource exists.

In this regard, attention is specifically directed to lines 18-23 on page 6 of applicants' specification which are reproduced below for convenience:

"Operating system level 200 typically manages resources such as memory 201 particularly in the form of virtual memory and also manages the CPU resource availability. Likewise, at hardware level 100, resources include such things as memory 101, disk storage or DASD 102, tape drive 104 and CPUs 103. The CPU management at operating system level 200 and hardware level 100 are not the same. This is why a resource such as

<u>CPUs is present at both the hardware and operating system levels.</u>" [Emphasis added herein.]

This excerpt from applicants' specification clearly indicates that a simple CPU is not just a single resource, but that a CPU can be treated differently as a resource depending upon the level (administrative vs. hardware, for example). These are the kinds of distinctions that are present in applicants' claimed invention. However, there is nothing seen in the patent to Jones et al. or in any of the other art cited by the Examiner which discloses or teaches the concept of computer resources at different levels. While the art cited may appreciate that various resources have various capacities, there is no teaching, disclosure, or suggestion that these capacities may be treated and accessed differently depending upon the level at which the request is made. However, in applicants' claimed invention, users are able to specify this level and, accordingly, achieve a degree of flexibility in job scheduling that has heretofore been unattainable in schedulers such as that described by Jones et al.

Since a rejection under 35 U.S.C. § 102 is a narrow ground of rejection requiring the presence of all claimed elements within the four corners of a single cited document, it is clearly seen that the patent to Jones et al. is deficient as a basis for rejecting applicants' claims. In particular, it is noted that the applicants' claims recite the utilization and designation of levels at which a resource may exist. In contrast, it is seen that this concept is not present in Jones et al. While Jones et al. may teach the existence of different types or capacities for their resources, the additional notion of level is not present. For example, it is seen that Jones et al. have no appreciation whatsoever that a CPU may be present as a different resource at the hardware level than at the administrative or operating system levels.

Accordingly, since the concept of "level" is absent from the teachings of Jones et al., it is seen that this patent cannot be employed as a basis for rejecting claims which specifically and positively recite the use of levels. For this reason, it is seen that the rejection of applicants' Claims 1-4 cannot be sustained. It is therefore respectfully

requested that the board reverse the Examiner and allow all of appellants' recited claims.

With specific reference to applicants' Claim 4, the other independent claim considered herein, it is noted that this claim also contains a positive recitation of a level, type, and quantity description. As such, it too recites aspects not present in the patent to Jones et al.

B. Rejection Under 35 U.S.C. § 112

While the Examiner has made no indication as to the status of applicants' claims with respect to the previous rejection under 35 U.S.C. § 112, it is submitted herein that applicants' amendments, as specified in the aforementioned response under 37 C.F.R. § 1.116, is in full compliance with the Examiner's previously stated objections to the claim language. Accordingly, it is asserted that the claims as listed herein are in full compliance with 35 U.S.C. § 112. It is therefore respectfully requested that to whatever extent necessary, the Examiner's rejection of applicants' claims under 35 U.S.C. § 112 be reversed. This reversal is therefore respectfully requested.

IX. CONCLUSION

Appellants respectfully request reversal of each of the rejections set forth in the final action. Appellants submit that their claimed invention would not have been anticipated nor would it have been rendered obvious in view of the cited art. Applicants' further assert that their recited concept of "levels" is completely absent from the art cited. Appellants further assert that their claims as presented below are also in full compliance with 35 U.S.C. § 112. Accordingly, for all of these above reasons, appellants allege error in rejecting their claims. Reversal of all of the rejections is therefore respectfully requested.

X. APPENDIX

1. A method for managing resources in a multiprocessor data processing system, said method comprising the steps of:

defining to multiprocessors in said data processing system at least one resource, together with a quantity and type associated with that resource, said quantity being indicative of resource capacity, said resource also having a level selected from the group consisting of hardware level, operating system level, administrative system level and application level;

determining whether an application level user has requested use of said at least one resource;

determining availability, among said multiple processors, of said requested resource as to level, type and quantity; and

dispatching a user job which requests said resource upon the condition that said determining of availability indicates that said resource is available at the level and in the type and quantity requested.

- 2. The method of claim 1 in which said hardware level includes resources selected from the group consisting of CPUs and random access memory.
- 3. The method of claim 1 in which said operating system level resource includes virtual memory.
- 4. A method for providing an application level user with control of a data processing system having multiple processors, said method having the steps of:

analyzing user supplied command statements which provide access to resources having internal resource models, said resource models including, for each resource, a level, type and quantity description, wherein at least one resource model is defined consistently among said multiple processors, said level being selected from the group consisting of hardware level, operating system level, administrative level and application level; and

interpreting said command statements so that user jobs are scheduled to run and to use resources specified by said command statements.

RESPECTFULLY SUBMITTED

Date: May 17, 2004

By:

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